(b) a semiconductor chip mounted on the front side of the substrate, the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

A1 cont.

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias, these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

(g) an electrically-conductive bridge as a bonding wire that spans in an overhead manner across the interposing electrically-conductive trace such that the bonding wire is free of interference with the interposing electrically-conductive trace, wherein the bonding wire has one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

7. (Amended) The BGA package of claim 6, wherein the bonding wire is mounted through wire-bonding technology.

8. (Amended) The BGA package of claim 6, wherein the bonding wire is a gold wire.

Please **cancel** claims 9 and 10 without prejudice or disclaimer.

Please **add** the following new claims:

A2

11. (New) A BGA (ball grid array) package, which comprises:

(a) a substrate having a front side and a back side;

(b) a semiconductor chip mounted on the front side of the substrate, the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias, these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

A2 cont.

(g) an electrically-conductive bridge as a chip resistor that spans in an overhead manner across the interposing electrically-conductive trace such that the chip resistor is free of interference with the interposing electrically-conductive trace, wherein the chip resistor has one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

12. (New) The BGA package of claim 11, wherein the chip resistor is mounted through SMT technology.

13. (New) The BGA package of claim 11, wherein the chip resistor is a low-resistance chip resistor.

and B4

REMARKS

Claims 1-8 and 11-13 are pending in the application. Claims 1-5 have been withdrawn from consideration as being drawn to a non-elected invention. Claims 6-8 have been amended, claims 9 and 10 have been canceled without prejudice or disclaimer, and new claims 11-13 have been added by the present amendment.

As an initial matter, the title has been amended to clearly reflect the invention to which the elected claims are drawn. It is respectfully requested that the objection to the title be withdrawn.